# QRSS-8P-1800

## 0.4–1.8 GHz Direct Down-Conversion RF Front-End

### DESCRIPTION

The QRSS-8P-1800 is a fully integrated, reconfigurable switch-capacitor mixer-first RF receiver front-end operating from 0.4 to 1.8 GHz. Using an innovative eight-path quarter-rate subsampling (QRSS) architecture, it achieves direct (zero-IF) down-conversion and wideband 50-Ω impedance matching simultaneously—without an external LNA.

The device exploits the third harmonic of the QRSS sampling clock ($f_s$) and an eight-path passive mixer transparency property to translate the 50-Ω antenna impedance directly to the RF port. The sampling frequency is three times lower than the input RF frequency, dramatically reducing VCO and clock-distribution power by up to 89% versus conventional RF-sampling architectures.

Implemented in 65 nm CMOS process and occupying only 0.32 mm², the QRSS-8P-1800 is ideally suited for battery-powered IoT nodes, smart utility networks, rail communications, healthcare wearables, and software-defined radio platforms requiring sub-6 GHz multi-standard coverage.

### KEY FEATURES

- Frequency range: 0.4–1.8 GHz
- Direct (zero-IF) quadrature down-conversion
- Eight-path passive CMOS switch-capacitor mixer
- No external Matching required — 50-Ω input match at mixer
- Sampling frequency 3× lower than RF (89% VCO power saving vs. RF sampling)
- Noise Figure: 4.7 dB
- Conversion Gain: 22 dB
- IB-$IIP_3$: −1 dBm | OB-$IIP_3$: +8 dBm
- 3-dB Bandwidth: 90 MHz
- Mixer power: 800 µW
- BBLNA power: 23 mW
- Active area: 0.32 mm² in 65 nm CMOS
- Supply voltage: 1.2 V (core)

## APPLICATIONS

| Application | Relevant Bands | Notes |
|---|---|---|
| **Smart Utility Networks (SUN)** | 400–900 MHz | Long battery life, sub-GHz LPWAN |
| **Rail Communications & Control (RCC)** | 400–900 MHz | Robust wideband reconfigurability |
| **Healthcare & Body-Area Wearables** | 400 MHz, 915 MHz, 2.4 GHz* | Ultra-low mixer power (800 µW) |
| **Industrial IoT Monitoring** | Sub-1 GHz / ISM 2.4 GHz* | Wide-band, low-power platform |
| **Cellular Band Scanning / CAT-M** | 700–1800 MHz | Direct down-conversion, no IF filter |

## ELECTRICAL SPECIFICATIONS

*TA = 27°C, VDD = 1.2 V, unless otherwise noted.*

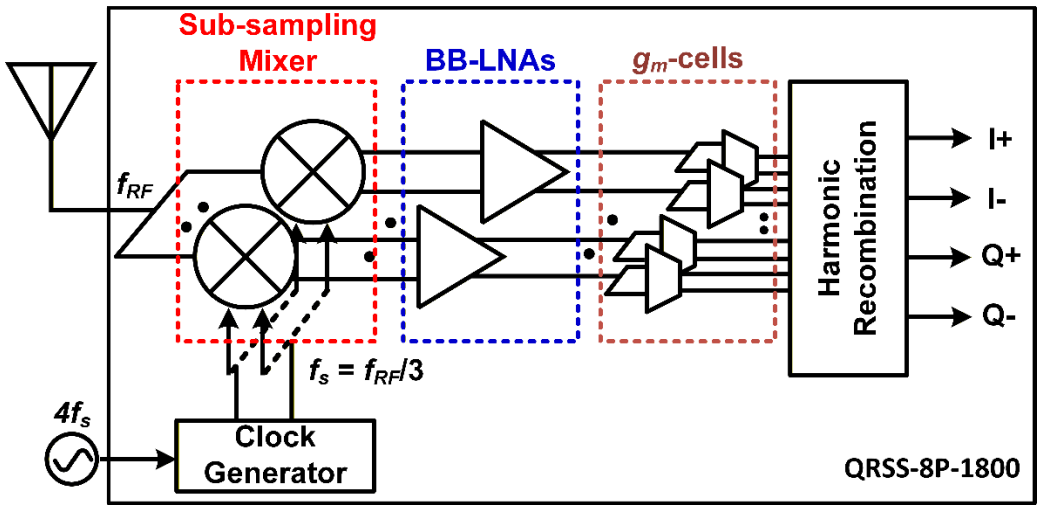
| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| **RF Frequency Range** | $f_{RF}$ | 0.4 | — | 1.8 | GHz | |
| **Sampling Frequency** | $f_s$ | 0.13 | — | 0.6 | GHz | |
| **Noise Figure** | NF | 4.7 | — | 8.0 | dB | 0.4 – 1.8 GHz band |
| **Conversion Gain** | G | — | 22 | — | dB | ±1.5 dB variation over band |
| **3-dB Bandwidth (Baseband)** | BW | — | 90 | — | MHz | $f_{RF}$ = 1.47 GHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| **In-Band $IIP_3$** | IB-$IIP_3$ | — | −1 | — | dBm | Δf = 1 MHz |
| **Out-of-Band $IIP_3$** | OB-$IIP_3$ | — | +8 | — | dBm | Δf = 150 MHz |
| **Input P1dB** | IP1dB | — | −15 | — | dBm | $f_{RF}$ = 1.47 GHz |
| **Input Return Loss (at $3f_s$)** | $S_{11}$ | -35 | −20 | −10 | dB | Matched to 50 Ω |
| **Harmonic Rejection (1st)** | $HR_1$ | — | 36 | — | dB | vs. 3rd harmonic |
| **Supply Voltage (Core)** | VDD | — | 1.2 | — | V | |

## POWER CONSUMPTION

| Block | Power | Supply | Notes |
|---|---|---|---|
| **Eight-Path Subsampling Mixer** | 800 µW | 1.2 V | Constant over 0.4–1.8 GHz |
| **Baseband LNA (BBLNA)** | 23 mW | 1.2 V | At Vcntrl = 0.4 V for $IIP_3$ = −1 dBm |
| **$g_m$-Cell** | 3 mW | 1.2 V | Harmonic recombination stage |
| **Nonoverlapping Clock Generator** | 2–9.2 mW | 1.2 V | Scales with $f_s$ (0.13–0.6 GHz) |

## ARCHITECTURE OVERVIEW




### Signal Path

- Off-chip RF band-select filter suppresses blockers at odd harmonics of $f_s$
- Eight-path 12.5%-duty-cycle passive switch-capacitor mixer down-converts RF at the 3rd harmonic of $f_s$ directly to zero-IF
- Differential CMOS inverter-based noise-cancelling BBLNA provides gain and baseband impedance
- $g_m$-cells duplicate and amplify BB outputs for harmonic recombination
- Harmonic recombination extracts I/Q at $3f_s$ and attenuates 1st- and 5th-harmonic spurs

### Impedance Matching

- No external IF matching network required—simplifies PCB layout
- $S_{11}$ < −10 dB maintained across full 0.4–1.8 GHz band

## FREQUENCY PLAN

| Parameter | Formula / Value | Example ($f_{RF}$ = 1.47 GHz, k = 1) |
|---|---|---|
| **Sampling Frequency ($f_s$)** | $f_{RF}$ / (2k + 1) \| k = 1, 2, 3… | 490 MHz |
| **Effective LO Frequency ($3f_s$)** | 3 × $f_s$ | 1.47 GHz |
| **Baseband Frequency ($f_{BB}$)** | $f_{RF} - n \cdot f_s$ \| n = 1, 3, 5… | 20 MHz (n = 3) |

## ABSOLUTE MAXIMUM RATINGS

*Stress above listed limits may permanently damage the device. Functional operation at these limits is not implied.*

| Parameter | Limit | Unit |
|---|---|---|
| **Core Supply Voltage (VDD)** | 1.2 + 0.3 | V |
| **I/O / Buffer Supply Voltage** | 2.5 + 0.5 | V |
| **Operating Temperature** | −40 to +85 | °C |
| **ESD Rating (HBM)** | 2000 | V |

## DEVICE INFORMATION

| Parameter | Value |
|---|---|
| **Part Number** | QRSS-8P-1800 |
| **Technology** | 65 nm CMOS (TSMC 1P9M) |
| **Die Size (Active)** | 0.32 mm² |
| **Die Supply (Core)** | 1.2 V |
| **Die Supply (I/O)** | 2.5 V |
| **Package** | QFN40 |
| **Operating Temperature Range** | −40°C to +85°C |

## DESIGN SUPPORT & RELATED RESOURCES

For more information, visit www.Chipinsemi.com All product names, logos, and brands are property of their respective owners