NEUROCORE

Energy-Efficient Neuromorphic Building Blocks for Extreme Edge IoT Applications

DESCRIPTION

NEUROCORE is a collection of energy-efficient CMOS neuromorphic building blocks for Extreme Edge IoT applications. Implemented in TSMC 65 nm CMOS technology, the platform includes ultra-low-power silicon neuron, STDP-based synapses, and associative memory circuits. The proposed circuits support biologically inspired spiking and learning mechanisms while operating at very low supply voltages and power levels.

The developed neuron circuits achieve energy consumption as low as 3.5 pJ/spike at 0.5 V. The STDP synapse enables on-chip learning with 1.2 pJ per learning event, while the associative memory consumes only 800 pW average power. NEUROCORE has been fabricated through ASIC tape-out in TSMC 65 nm CMOS technology and serves as a foundation for future neuromorphic processors and Edge AI systems.

KEY FEATURES

- 65 nm CMOS Technology
- PBXCIP Neuron: 3.5 pJ/spike @ 0.5 V
- Spiking Frequency: 30 Hz
- Neuron Area: 58 µm × 42 µm
- STDP Synapse: 1.2 pJ/learning event
- Associative Memory: 800 pW average power
- Associative Memory Area: 150 µm × 65 µm
- On-Chip STDP Learning
- Extreme Edge AI & IoT Applications

APPLICATIONS

Application	Notes
Wearable Healthcare Sensors	Biological signals (ECG, EEG, EMG) are low frequency and battery-powered
Implantable Biomedical Devices	Ultra-low power is critical for long battery life
Environmental Monitoring Sensors	Event-driven sensing with very low data rates
Always-On Wake-Up Systems	Continuous monitoring with minimal power
Edge IoT Sensor Nodes	Battery-operated event-driven intelligence

PERFORMANCE SPECIFICATIONS

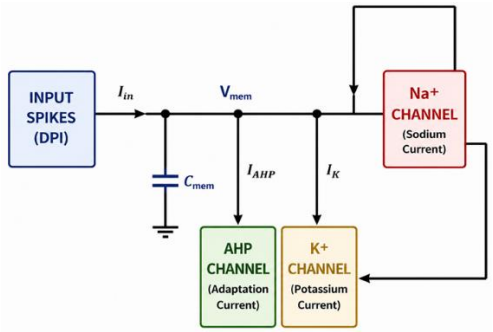
TA = 27°C, VDD = 0.5 V, unless otherwise noted.

Parameter	Symbol	Value
Spiking Frequency	f_s	30 Hz
Energy per spike	E_s	3.5 pJ
Supply Voltage (Core)	VDD	0.5 V

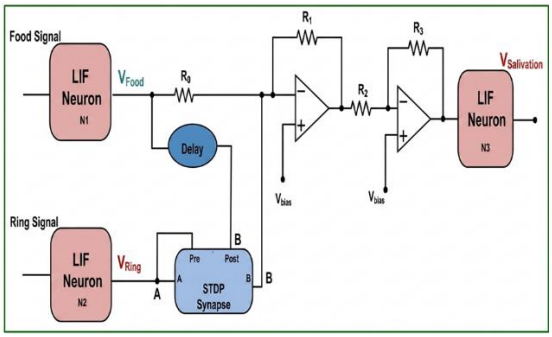
POWER / ENERGY CONSUMPTION

Block	Power / Energy	Supply
PBXCIP Neuron	3.5 pJ	0.5 V
STDP Circuit	1.2 pJ	0.5 V
Associative Memory	800 pW	0.5 V

ARCHITECTURE OVERVIEW



Block diagram of DPI-based silicon neuron circuit



Block diagram of Associative Memory

Silicon Neuron

- Integrates input spikes and generates action spikes.
- Supports spike-frequency adaptation through AHP feedback.
- Ultra-low-power operation for neuromorphic computing.
- Mimics key behavior of biological neurons.

Associate Memory

- Built using 3 LIF neurons, 1 STDP synapse, and a delay block.
- Learns associations using spike-timing-dependent plasticity (STDP).
- Demonstrates Pavlovian associative learning.
- Enables low-power on-chip learning and memory.

DEVICE INFORMATION

Parameter	Value
Part Number	NEUROCORE
Technology	TSMC 65 nm CMOS (1P9M)
Die Size (Active)	0.188 mm^2
Die Supply (Core)	0.5 V
Operating Temperature Range	−10°C to +50°C

DESIGN SUPPORT & RELATED RESOURCES

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