SALLPHC

Energy-Efficient Hybrid Circuit Design for Full-Duplex Communication

DESCRIPTION

High-speed full-duplex chip-to-chip communication enables simultaneous bidirectional data transfer over a single interconnect. Consequently, a hybrid circuit is required to separate the received signal from the interconnect signal effectively.

Therefore, a strong-arm latch hybrid has been designed that operates at 12 Gb/s full-duplex communication.

Implemented in 65 nm CMOS technology, the design operates at 12 Gb/s full duplex communication. The design also demonstrates low power, low timing jitter, a low bit-error rate, and reliable performance over a 20 cm FR4 PCB trace.

KEY FEATURES

- 65 nm CMOS Technology
- Data rate: 12 Gb/s full duplex
- Frequency: 3 GHz
- Half-rate clock operation
- Eliminate the equalizer circuit
- Strong-arm latch Hybrid power: 3.86 mW
- Active area: 0.4 mm^2
- Supply voltage: 1.2 V (core)

APPLICATIONS

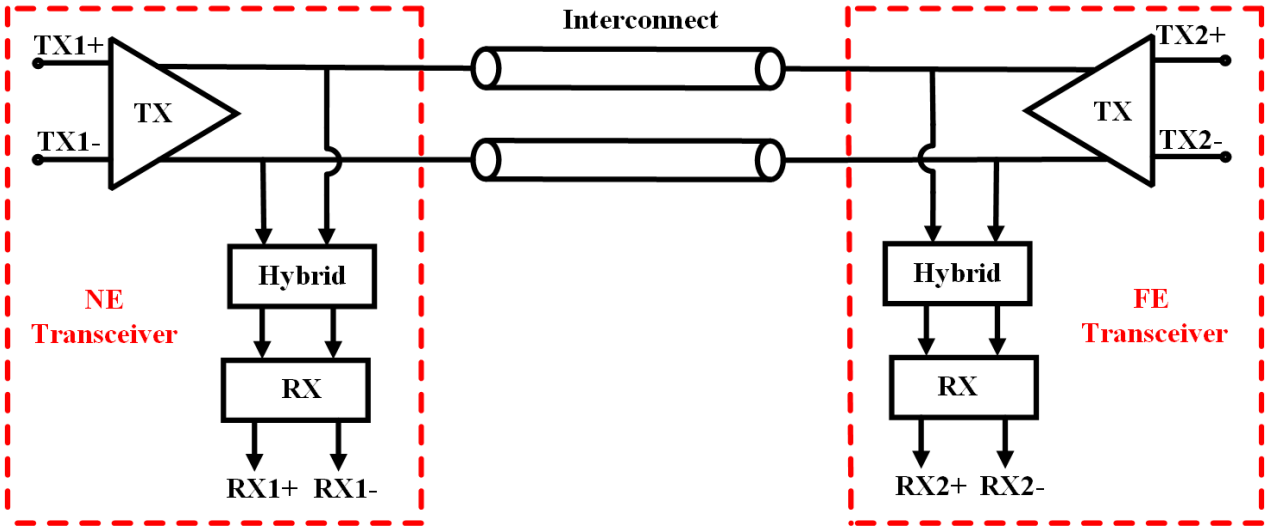
Application	Notes
High-speed, low-power data transfer	Energy-efficient short-reach communication
Multi-chip module interface	Die-to-die communication within multi-chip modules
Memory and storage interface	Communication between the processor and memory

PERFORMANCE SPECIFICATIONS

TA = 27°C, VDD = 1.2 V, unless otherwise noted.

Parameter	Value
Frequency	3 GHz
Channel Loss	4.9 dB
Eye Opening	460 mV
Power Consumption	3.86 mW
Energy Efficiency	0.32 pJ/bit
Bit Error Rate	10^{-12}
Supply Voltage	1.2 V

ARCHITECTURE OVERVIEW



Full-duplex communication

- Simultaneous bidirectional data transmission over a 20 cm off-chip interconnect
- Differential signalling to improve the signal integrity

Hybrid architecture description

- Power consumption is low
- provide rail-to-rail output
- eliminate the equaliser circuit
- Reduce circuit complexity

DEVICE INFORMATION

Parameter	Value
Part Number	SALLPHC
Technology	65 nm CMOS (TSMC 1P9M)
Die Size (Active)	0.4 mm²
Die Supply (Core)	1.2 V
Operating Temperature Range	−20°C to +100°C

DESIGN SUPPORT & RELATED RESOURCES

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