DC-03 | Common Mode insenstivie Low-Power and Low-Noise Dynamic Comparator

DC-03

Energy-Efficient Mixed-Signal Circuits

DESCRIPTION

Dynamic Comparator (DC-01) is a 1.2 V low-power dynamic comparator designed to generate rail-to-rail digital outputs with a differential input sensitivity of 1 mV. The comparator operates over a supply voltage range of 0.9 – 1.2 V and supports a common-mode input voltage range of 0.5 – 1.2 V. The proposed architecture is optimized for low-power and low-noise operation, making it suitable for high-performance analog-to-digital converter (ADC) applications.

The dynamic comparator achieves an energy consumption as low as 43 fJ per comparison, a clock-to-output delay of 1.2 ns, and an input-referred noise of 0.3 mV. Implemented in a 65 nm CMOS process and occupying an area of only 100 µm², DC-02 is well suited for low-power and high-speed mixed-signal systems, including SAR ADCs, healthcare wearables, battery-powered IoT devices, wireless communication systems, high-speed serial links, and edge IoT sensor nodes.

KEY FEATURES

- 65 nm CMOS Technology
- Rail-to-rail input
- Wide supply range: 0.9 – 1.2 V
- Frequency: 25 MHz
- Energy per comparison: 43 fJ
- CLK to OUT Delay: 1.2 ns
- Input Referred Noise: 0.3 mV
- Extreme Edge AI & IoT Applications

APPLICATIONS

Application	Notes
Biomedical Systems	Used in ECG and EEG instruments which requires low noise
Wearable and Health Monitoring Devices	Ultra-low power and high sensitivity is critical for long battery life
Wireless Communication Systems	Used for ADCs and signal processing circuits inside the receiver
SAR ADCs and Noise-Shaping ADCs	used as decision making block in ADCs
High Speed Serial Links	Performs data slicing and rapid symbol detection in receiver circuits
Edge IoT Sensor Nodes	Interfaces with sensors outputs and converting them into digital to support long battery life

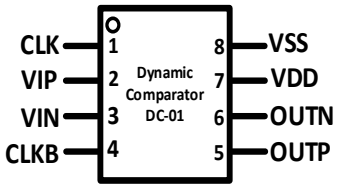
PERFORMANCE SPECIFICATIONS

TA = 27°C, VDD = 1.2 V, unless otherwise noted.

Parameter	Symbol	Value
Frequency	f_s	25 MHz
Sensitivity	S	1 mV
Energy per comparison	E	43 fJ
CLK to OUT Delay	D	1.2 ns

Input Referred Noise	IRN	0.3 mV
Supply Voltage (Core)	VDD	1.2 V

PIN Configuration and Description



PIN Diagram

CLK : Clock input
CLKB : Clock bar input
VIP : Non Inverting input
VIN : Inverting input
OUTP : Non Inverting output
OUTN : Inverting output
VDD : Supply voltage
VSS : Supply ground

ABSOLUTE MAXIMUM RATINGS

Stress above listed limits may permanently damage the device. Functional operation at these limits is not implied.

Parameter	Limit	Unit
Core Supply Voltage (VDD)	1.2 + 0.2	V
I/O / Buffer Supply Voltage	1.2 + 0.2	V
Operating Temperature	−40 to +75	°C
ESD Rating (HBM)	2000	V

DEVICE INFORMATION

Parameter	Value
Part Number	Dynamic Comparator
Technology	TSMC 65 nm CMOS (1P9M)
Die Size (Active)	100 μm^2
Die Supply (Core)	1.2 V
Die Supply (I/O)	1.2 V
Operating Temperature Range	−10°C to +50°C

DESIGN SUPPORT & RELATED RESOURCES

For more information, visit https://www.linkedin.com/company/chipinsemi/ All product names, logos, and brands are property of their respective owners